REMARKS

Claims 1-26 are all the claims presently pending in the application. Claims 1, 14 and 26 have been amended to more clearly define the invention. Claims 2-13 and 15-25 have been withdrawn from prosecution. Of the remaining claims, claims 1, 14 and 26 are independent.

These amendments are made only to more particularly point out the invention for the Examiner and not for narrowing the scope of the claims or for any reason related to a statutory requirement for patentability.

Applicant also notes that, notwithstanding any claim amendments herein or later during prosecution, Applicant's intent is to encompass equivalents of all claim elements.

Claims 1, 14 and 26 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kawamoto, et al. (U.S. Patent No. 5,453,994) in view of Giedd et al. (U.S Patent No. 3,614,608).

This rejection is respectfully traversed in the following discussion

I. THE CLAIMED INVENTION

The claimed invention is directed to a semiconductor device tester which includes an electron beam gun, a current measurer, a memory and a comparator. The electron beam gun irradiates each of a plurality of test samples with an electron beam. The current measurer measures current generated on a back surface of each of the plurality of test samples by the electron beam. The memory stores current waveforms for each of the plurality of test samples. The current waveforms are variations of the measured current for each of the plurality of test samples in correspondence with irradiation positions of the electron beam on

each of the plurality of test samples. The comparator compares the current waveforms and, when a difference between the current waveforms exceeds a predetermined value, outputs information related to the position on one of the plurality of test samples at which the difference exists.

As mentioned in the previous Amendment, the present invention, provides a test device and method which provides results without relying upon CAD data. Rather, the present invention generates data from each of a plurality of test samples and compares that data to determine when one of those test samples is defective (see, for example, page 2 line 17 - page 3, line 3). In this manner, the present invention avoids any need to generate data based upon a design. Instead, the present invention is capable of determining defects by comparing results between test samples to determine whether a defect exists (see, for example, page 3, lines 4-10).

The present invention is also capable of determining defects among randomly arranged devices without reference to CAD data. Additionally, the present invention obviates the need to transfer data between devices.

II. THE PRIOR ART REJECTION

Regarding the rejection of claims 1, 14 and 26, the Examiner alleges that the Giedd et al. reference would have been combined with the Kawamoto et al. reference to form the claimed invention. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Applicant submits that these references would not have been combined as alleged by

the Examiner. Indeed, the references are directed to completely different matters and problems.

Specifically, the Kawamoto et al. reference is directed to providing an improved semiconductor test system. In particular, the Kawamoto et al. reference discusses the problems of conventional semiconductor test systems which rely upon responses from output pads to test signals provided to input pads (col. 1, lines 10-56 and Fig. 6). The Kawamoto et al. reference teaches substituting a tester which relies upon an optical beam induced current measuring device rather than a conventional hard wiring to input pads to provide a test signal to the semiconductor circuit (col. 1, line 60 - col. 2, line 6).

In contrast, the Giedd et al. reference is directed to improving the testing of highly complex logic circuits which rely upon responses from output pads to predetermined test patterns provided to input pads (col. 1, lines 15-37) by substituting a random test pattern for the predetermined test patterns (col. 1, lines 46-48). One of ordinary skill in the art would not have been motivated to modify the optical beam induced current measuring device disclosed by the Kawamoto et al. reference based upon the test system which relies upon providing test patterns to input pads as disclosed by the Giedd et al. reference. Thus, the references would not have been combined, absent hindsight.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner does not even support the combination by identifying a reason for combining the references.

The Examiner alleges that it would have been obvious for one of ordinary skill in the art to replace the expected values 5b disclosed by the Kawamoto et al. reference with the physical reference test sample disclosed by the Giedd et al. reference "since this is an

alternative way to obtain the expected values by using a physical reference device." However, assuming arguendo that these are alternatives, the mere fact that these are alternatives does not provide any motivation or suggestion for making the proposed modification. A prima facie case of obviousness requires that the applied references provide a motivation and/or suggestion for making the alleged modification. The mere presentation of an alternative does not provide any motivation or suggestion to make a substitution.

Further, the Examiner's alleged modification would not arrive at the claimed invention. The Examiner alleges that it would have been obvious to substitute the expected values 5b disclosed by the Kawamoto et al. reference with the physical reference test sample as disclosed by the Giedd et al. reference. However, the claims recite a memory means that stores current waveforms for each of a plurality of test samples and a comparator means which compares those waveforms. If one were to make the modification suggested by the Examiner, the alleged modification would not provide either of these features.

The Giedd et al. reference teaches simultaneously testing two physical devices and comparing the outputs from both of those devices. Therefore, if one were to rely upon the Giedd et al. reference to find a modification to the Kawamoto et al. reference, as alleged by the Examiner, and assuming arguendo that there was a motivation and/or a suggestion to do so, one of ordinary skill in the art would no longer rely upon storing the current waveforms before comparing them. Rather, one would merely compare the waveforms as they were output from the test sample and the reference test sample. Otherwise, there would be no need to provide a physical reference test sample.

Further, such a modification of requiring a comparison between two physical devices, as taught by the Giedd et al. reference would increase the complexity and cost of the test

system disclosed by the Kawamoto et al. reference.

Moreover, even assuming arguendo that one of ordinary skill in the art would have been motivated to combine these references, the combination would not teach or suggest each and every element of the claimed invention.

The Kawamoto et al. reference discloses a semiconductor test system which combines the features of a conventional tester 5, which analyzes a semiconductor device based upon signals received on output pads 2b in response to signals applied to input pads 2a, with a measuring device 8, which analyzes the device based upon signals generated in response to laser irradiation. However, as agreed during the March 10, 2003 personal interview, the Kawamoto et al. reference does not teach or suggest the features of independent claims 1 and 14 including: 1) a memory that stores current waveforms from a back surface of each of a plurality of test samples; and 2) a comparator that compares those current waveforms. In other words, the present invention compares stored current waveforms of each of a plurality of test samples.

To the contrary, the Kawamoto et al. reference is similar to the conventional measuring devices described in the present specification because the Kawamoto et al. reference also relies upon a comparison between data received by the test sample and data which was generated based upon CAD generated data.

Like the conventional art, the Kawamoto et al. reference compares data from the test sample with an "expected value" data (see, for example, col. 2, lines 34-35; col. 4, lines 55-61; col. 5, lines 1-2). The Kawamoto et al. reference does not disclose the source of that "expected value" data. Indeed, the Kawamoto et al. reference only discloses that either an optical beam induced current (OBIC) is received or not. The Kawamoto et al. reference

discloses using only a binary bit to determine whether an OBIC is either detected (1) or not detected (0) (col. 5, line 46 - col. 6, line 12; Table 1 and Fig. 2.). Binary data of "expected values" like that are easily obtained using CAD data and does not even require an approximation of a current waveform.

As explained above, the present invention provides a test device and method which stores data from each of a plurality of test samples and compares that data (e.g., waveform data of a first sample with waveform data of a second sample-not a predetermined reference value) to determine when one of those test samples is defective (see, for example, page 2 line 17 - page 3, line 3).

In this manner, the present invention avoids any need to generate data based upon a design. Instead, the present invention is capable of determining defects by comparing results between stored waveforms from each of a plurality of test samples to determine whether a defect exists (see, for example, page 3, lines 4-10).

Clearly, the Kawamoto et al. reference does not disclose comparing data stored from each of a plurality test samples to determine whether one of those test samples is defective in accordance with the invention. As a result, the Kawamoto et al. reference is not capable of providing the advantages of the present invention discussed above.

Further, the Kawamoto et al. reference teaches away from the type of testing device disclosed by the Giedd et al. reference. In 1971 the Giedd et al. reference discloses a logic testing circuit which relies upon inputting a signal into input pads and measuring the output received on output pads to measure the response of a circuit to an input signal. The response received from a logic circuit being tested was then compared to a physical reference logic circuit.

By contrast, in 1995 the Kawamoto et al. reference teaches away from the type of logic testing circuit disclosed by the Giedd et al. reference of providing an input signal to input pads and measuring the output from the output pads. The Kawamoto et al. reference explains that as an integrated circuit becomes larger in scale and higher in integration that the number of test patterns which are required for this type of test system must be increased substantially. The Kawamoto et al. reference also explains that it may be impossible to detect some types of defects using the type of test system which is disclosed by the Giedd et al. reference (col. 1, lines 43-56). Therefore, one of ordinary skill in the art would not have been motivated to modify the Kawamoto et al. reference based upon the teaching of the Giedd et al. reference because the Kawamoto et al. reference teaches away from the type of system disclosed by the Giedd et al. reference.

Moreover, the Giedd et al. reference, like the Kawamoto et al. reference, does not teach or suggest: 1) a memory that stores current waveforms for each of a plurality of test samples; and 2) a comparator that compares those current waveforms. As explained above, these features are important for determining defects among randomly arranged devices without reference to CAD data. Additionally, the present invention obviates the need to transfer data between devices.

Rather, the Giedd et al. reference discloses improving the testing of highly complex logic circuits which rely upon responses from output pads to predetermined test patterns provided to input pads (col. 1, lines 15-37) by substituting a random test pattern for the predetermined test patterns (col. 1, lines 46-48). The Giedd et al. reference discloses receiving output signals from each of the physical devices and using a group of inverters, AND circuits, OR circuits and a polarity hold circuit determines whether an error exists due

to a discrepancy between the outputs of corresponding pins (col. 4, line 58 - col. 5, line 7 and col. 7, lines 1-47 and Fig. 4). The Giedd et al. reference does not teach or suggest any type of memory, let alone a memory which stores the current waveforms from a back surface of each of a plurality of test samples.

In stark contrast, the present invention provides: 1) a memory that stores current waveforms from a back surface of each of a plurality of test samples; and 2) a comparator that compares those current waveforms. As explained above, these features are important for determining defects among randomly arranged devices without reference to CAD data. Additionally, the present invention obviates the need to transfer data between devices

Clearly, these novel features are not taught or suggested by Kawamoto, either above or with the Giedd et al. reference.

Therefore, the Examiner is respectfully requested to withdraw this rejection of claims 1, 14 and 26.

Lastly, regarding the means plus function recitations, the Examiner has failed to interpret the claims to read on the structures or materials disclosed in the specification and "equivalents thereof." The Federal Circuit has made it clear that the Office is required to interpret means plus function language in accordance with 35 U.S.C. § 112, sixth paragraph (see M.P.E.P. §2106; *In re Donaldson*, 16 F.3d 1189, 1193 (Fed. Cir. 1994) and *In re Alappat*, 33 F.3d 1526, 1540 (Fed. Cir. 1994)). Clearly, the Examiner has failed to interpret the claims to read on the structures or materials disclosed by the present specification and "equivalents thereof."

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing amendments and remarks, Applicant respectfully submits that claims 1-26, all the claims presently pending in the Application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the Application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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James E. Howard
Registration No. 39,715

McGinn & Gibb, PLLC
8321 Old Courthouse Rd., Suite 200
Vienna, Virginia 22182
(703) 761-4100
Customer No. 21254